A 0.18-μm BICMOS 20-57 GHz ULTRA-WIDEBAND LOW-NOISE AMPLIFIER UTILIZING FREQUENCY-CONTROLLED POSITIVE-NEGATIVE FEEDBACK TECHNIQUE

A Thesis

by

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ABSTRACT

Silicon based complementary metallic oxide semiconductor (CMOS) and Bipolar Complementary Metal Oxide Semiconductor (BiCMOS) radio frequency integrated circuits (RFICs), including microwave and millimeter-wave (MMW), are attractive for wireless communication and sensing systems due to their small chip size and facilitation in system-on-chip integration. One of the most important RFICs is the low-noise amplifier (LNA).

The design of CMOS/BiCMOS wideband LNAs at MMW frequencies, especially those working across several decades of frequency, is challenging due to various issues. For instance, the device parasitic and inter-coupling between nearby elements in highly condensed chip areas limits the operating bandwidth and performance, and the conductive silicon substrates lead to the inevitable low quality factor of passive elements.

In this work, a MMW BiCMOS ultra-wideband LNA across 20 to 57 GHz is presented along with the analysis, design and measurement results. To overcome the upper-band gain degradation and improve the in-band flatness, a novel frequency controlled positive-negative (P-N) feedback topology is adopted to modify the gain response by boosting the gain at the upper-band while suppressing that at the lower-band. To reduce overall power consumption, the first and second stages of the amplifier are stacked between supply voltage and DC ground to utilize the same DC current. At the output of amplifier, a shunt-peaking load stage is utilized to achieve wideband output matching.

The designed ultra-wideband MMW LNA is fabricated in JAZZ 0.18-μm BiCMOS technology. It shows a measured power gain of 10.5 ± 0.5 dB, a noise figure between 5.1-7.0 dB, input and output return losses better than -10 and -15 dB, respectively, an input 1 dB compression point higher than -19 dBm, and an input third-order intercept point greater than -8 dBm. It dissipates 16.6 mW from 1.8 V DC supply and has a chip area of 700×400 μm^2.

DEDICATION

To my parents, my wife, and my baby boy...

ACKNOWLEDGEMENTS

I would like to thank my committee chair, Dr. Nguyen, for his guidance, encouragement and patience in directing this work. I am also grateful to my committee members, Dr. Sánchez, Dr. Kish and Dr. Mohanty, for their time and support throughout the course of this research.

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I would like to thank my parents for their love and encouragement during my many years in the graduate schools. Finally, I want to express my love and gratitude to my wife and son, for their love, support and the happiness that they brought me throughout my graduate studies.

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CHAPTER I

INTRODUCTION

This chapter starts with the background of MMW wideband LNA design in CMOS/BiCMOS technology. Then the existing MMW wideband LNA designs are reviewed with pros and cons. Finally, the organization of this thesis is elaborated.

1.1. Background

In the past decades, as CMOS/BiCMOS technology is scaled to nanometer range, the performance of silicon-based transistor is tremendously improved to the point where the f_t (current-gain cutoff frequency) and f_{max} (maximum oscillation frequency) of 90nm CMOS transistor, are both above 140 GHz. Silicon based RFIC design in millimeter waves become practical and affordable. Owing to the advantages of providing more spectrum, high-data-rate, low cost and small chip size, Silicon based RFICs for microwave and MMW band wireless communications become one of the most attractive research area.

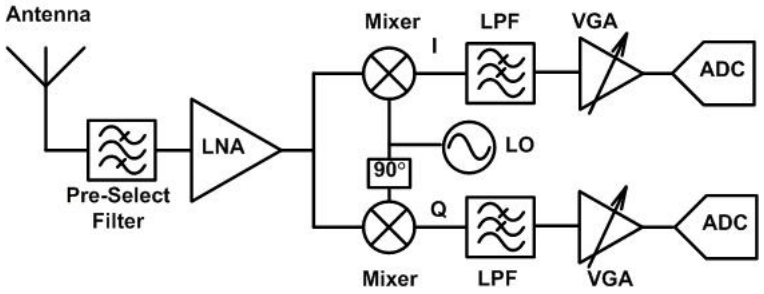


Figure 1 Block diagram of an RF receiver front-end

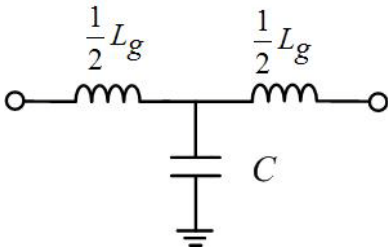
A typical block diagram of RF receiver front-end is shown in figure 1. Low noise amplifier (LNA) is one of the most important blocks in the front-end, which is placed after the antenna and pre-select filter to provide a sufficient gain to the received signal with minimized degradation of the signal-to-noise ratio (SNR). The key characteristics of wideband LNA's including sufficient high, flat gain, low noise figure, good input/output matching across the full band, linearity and power consumption, etc.

Silicon based wideband LNAs at millimeter-wave frequencies, especially those working across several decades of frequency, is challenging due to various issues such as device parasitic and inter-coupling between nearby elements in highly condensed chip area, that limit the operating bandwidth and performance, and the inevitable low quality factor of passive elements resulting from the conductive silicon substrates. Therefore, in wideband LNA design, different techniques are utilized to trade the design specifications between gain, bandwidth, and power consumption, etc.

1.2. Wideband Low Noise Amplifier Techniques

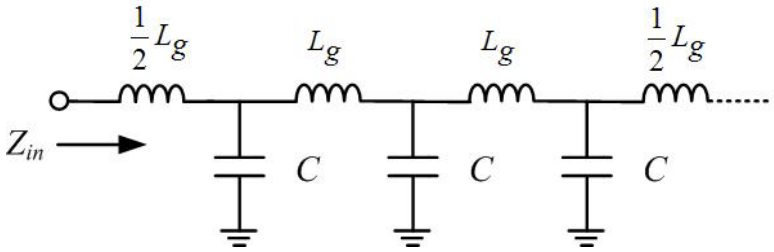
1.2.1. Distributed Amplifier

Distributed amplifiers are widely used in many wideband applications due to their intrinsic wideband characteristic. The basic design principle of distributed amplifiers is to form two 50-ohm artificial transmission lines at the input and output ports for wideband input and output matching purpose. While the combined multiple gain stages provide wideband gain up to the cut-off frequency of the artificial transmission line.



(a)

Figure 2 Lumped-element network representing unit section of artificial transmission line



(b)

Figure 3 An artificial transmission line consists of multiple series unit sections

A lumped element network is shown in figure 2. And the artificial transmission line comprised of multiple series connection of unite sections is shown in figure 3. The impedance of this artificial transmission line can be derived as:

$$Z_{in} \approx \frac{1}{2} j\omega L_g \pm \frac{1}{2} j\sqrt{\frac{L_g}{C}}\sqrt{\omega^2 L_g C - 4} \tag{1.1}$$

As frequency is increased to f_c, which has

$$f_c = \frac{1}{\pi\sqrt{L_g C}} \tag{1.2}$$

Z_{in} becomes $Z_{in} \approx j\sqrt{\frac{L_g}{C}}$, which is purely imaginary, hence no power can be delivered into amplifier input. f_c is so called the cutoff frequency of artificial transmission line.

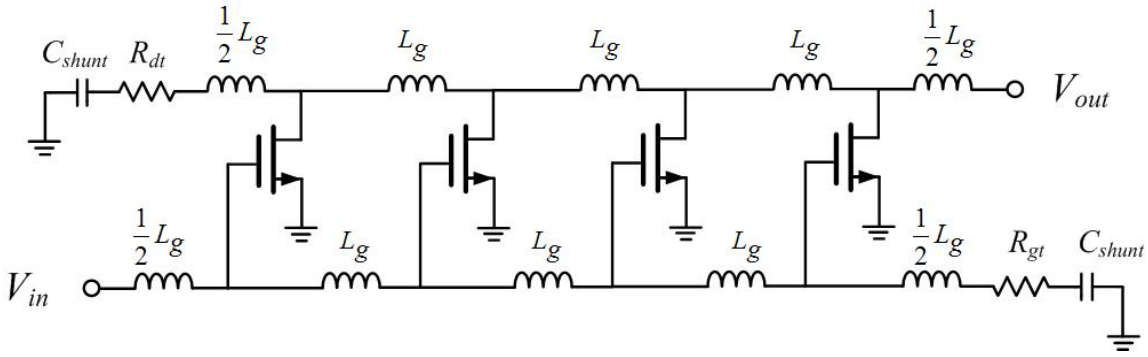


Figure 4 Schematic of 4-stage CMOS distributed LNA

Figure 4 shows a schematic of 4-stage distributed LNA using 90-nm silicon-on-insulator (SOI) technology in [1]. By absorbed the parasitic capacitors at gain and drain of MOSFETs into the input and output 50 ohms artificial transmission lines, this LNA achieves a flat gain of 9.7 dB ± 1.6 dB over a frequency range from 10 to 59 GHz. The NF is below 3.8 dB from 0.1 to 40 GHz. However, this distributed type amplifier has high power consumption of 132 mW due to the inherent nature of distributed structures, making it somewhat less desirable for wireless devices, particularly those for portable and mobile applications.

1.2.2. Amplifiers with Wideband Matching Network

A wideband amplifier topology with wideband input and output matching network is shown in figure 5. The wideband matching networks provide good input and output return loss across the operation frequency. A CMOS single-stage LNA using a 90-nm SOI technology is reported in [2]. It achieves a 3-dB bandwidth from 26 to 42 GHz with a peak gain of 11.9 dB and a minimum noise figure of 3.6 dB. However, the performance of this wideband amplifier is strongly affected by the on-chip low Q matching network, which makes it difficult to extend the operation bandwidth.

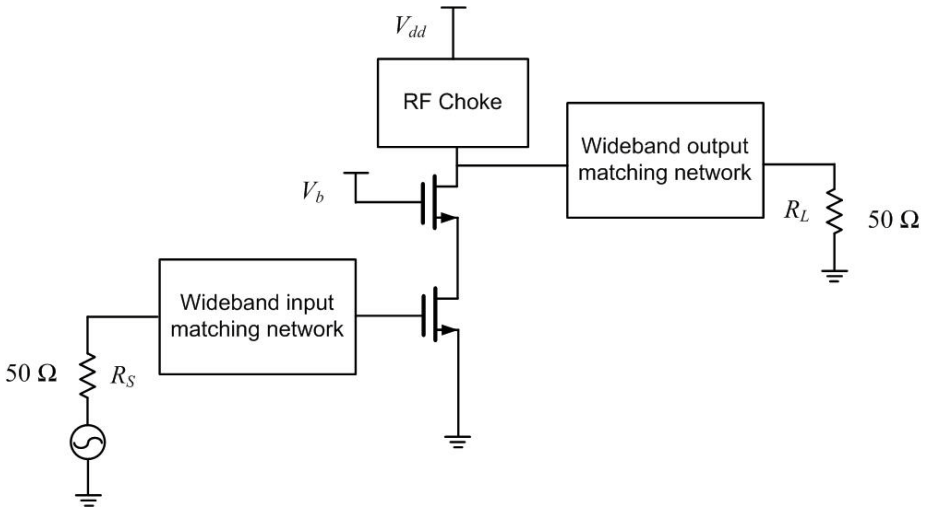


Figure 5 Simple amplifier schematic with wideband matching network

1.2.3. Multi-Cascode Wideband Amplifiers

Recently, multi-cascode CMOS LNAs become popular due to their high gain and compact size [3]-[5]. Several series resonant inductors in [3] and transformers in [4] are

placed between the common-gate (CG) devices to enhance the small-signal gain and improve noise figure. In figure 6, the V-band LNA in [3] using TSMC 65-nm process exhibits a 3-dB bandwidth from 47.7 to 61.3 GHz with 14.4 dB gain and a minimum noise figure of 4.5 dB at 54.6 GHz, under 10 mW power consumption. In figure 7, the V-band LNA in [4] using 90 nm process achieves a gain of 12.7 dB from 43 to 58 GHz and a minimum NF of 4.7 dB at 62.5 GHz with 18 mW power. However, a relatively high supply voltage of 3V is needed for these multi-cascode approaches.

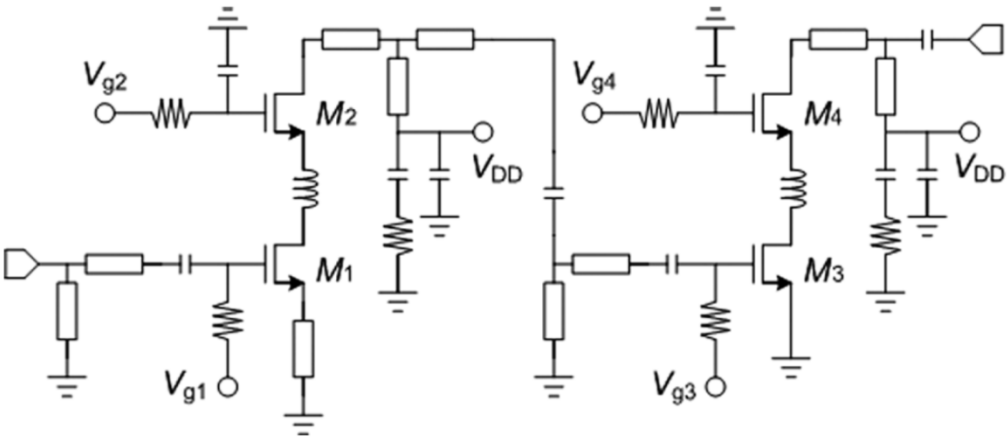


Figure 6 Multi-Cascode V-band LNA with noise-reduction inductor in [3]

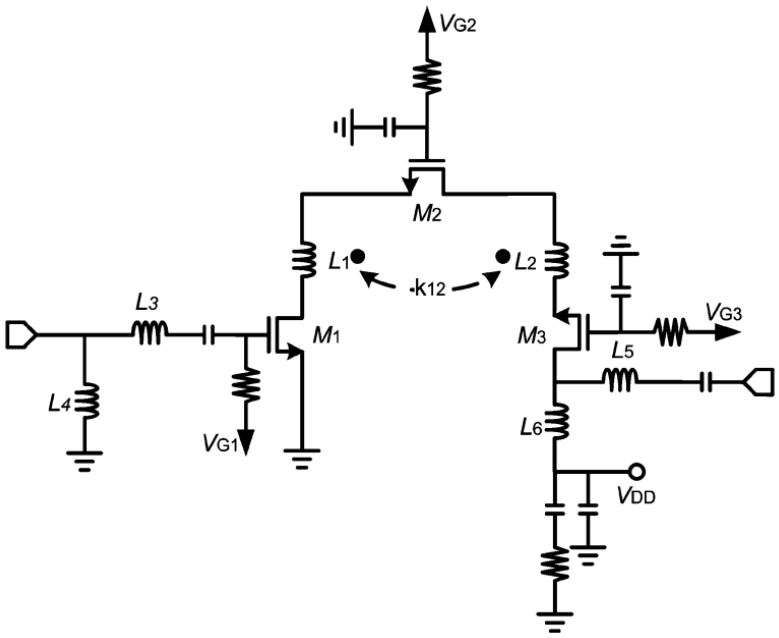


Figure 7 Multi-Cascode V-band LNA with noise-reduction transformer in [4]

To minimize the supply voltage, a magnetic coupled technique as shown in figure 8 is presented in [5] by implementing inter-stage transformers to couple the RF signal to the subsequent stages. With the 1.2V supply voltage and 14.4 mW power consumption, the triple-cascode LNA shows a 3-dB bandwidth from 49 to 60 GHz with peak gain of 13.7 dB and the lowest NF of 5.3 dB at 59.5 GHz. However, the LNA suffers bandwidth and NF degradation due to the parasitic and the low quality factor of the coupled transformers.

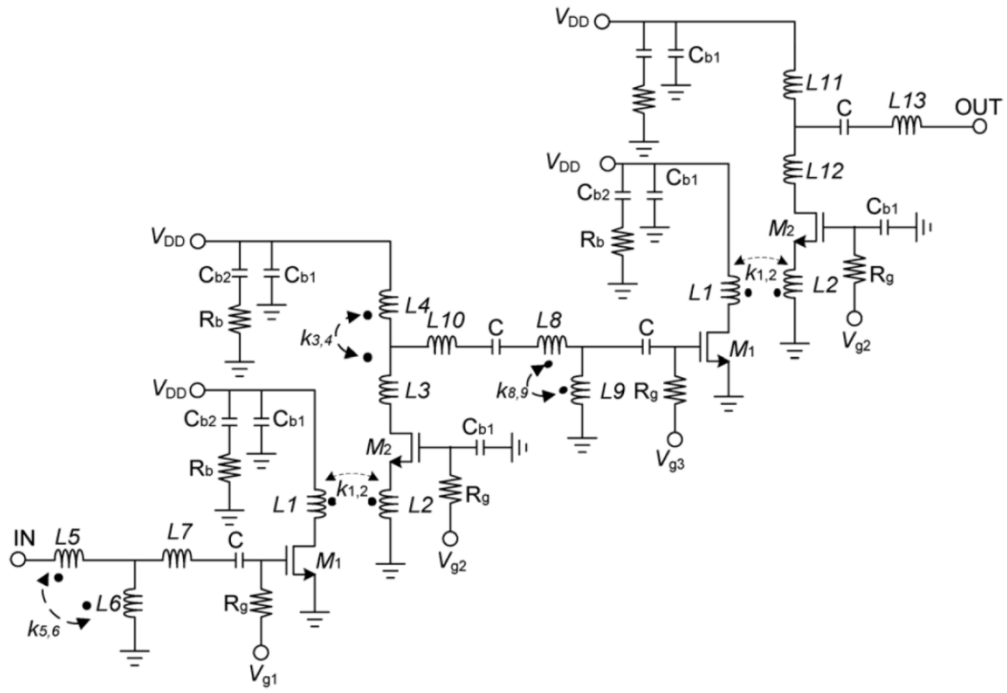


Figure 8 V-band LNA with magnetic coupled topology in [5].

1.2.4. Current-Reused Wideband LNA

Recently, LNAs based on current-reused technique for UWB application between 3 to 10 GHz have been reported [6]-[7]. By stacking two cascaded stages between supply voltage and ground as shown in figure 9, the transistors reuse the DC current. And the overall power consumption is only half of the conventional cascaded amplifier approach.

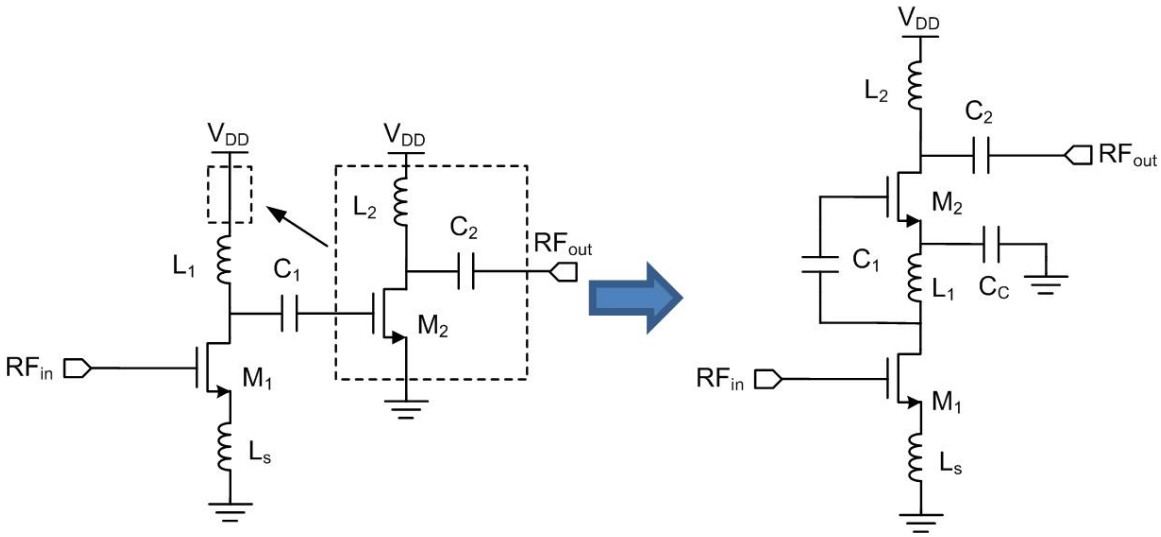


Figure 9 The concept of current-reused

Figure 10 shows that although each gain stage shows narrow-band characteristic, by arranging resonant frequencies of the load of two cascaded stages at the lower and upper band, respectively, an overall wideband gain response can be achieved. However, extending this technique to MMW frequency may not be suitable because the gain degradation caused by parasitic is serous as frequency increases. To enhance the upper-band gain and improve the in-band flatness, other techniques need to be employed.

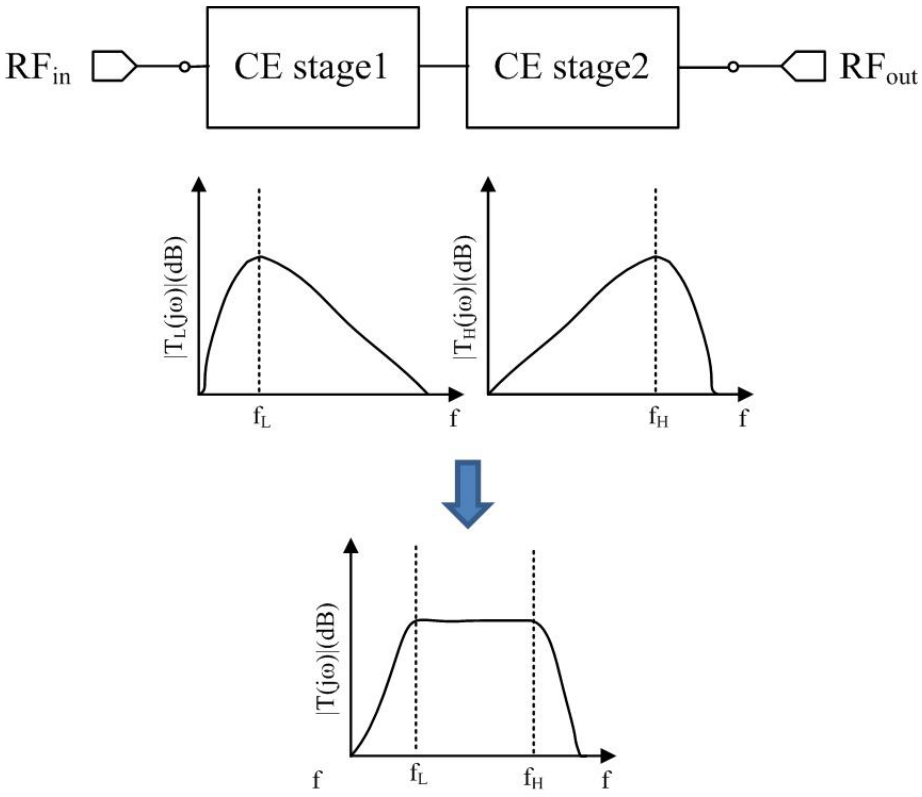


Figure 10 Overall wideband gain response from two cascaded stages

1.3. Organization

In this thesis, the fundamental concept and design consideration of wideband LNA is discussed in chapter II. Chapter III starts with the basic feedback theory and embedded positive-negative feedback. Then the frequency-controlled Positive-Negative feedback LNA along with analysis, simulation and experimental result is discussed. Finally, the conclusion is given in Chapter IV.

CHAPTER II

FUNDAMENTALS OF WIDEBAND LOW NOISE AMPLIFIERS

The key characteristics and design considerations for wideband LNAs are similar to those of narrow-band LNAs. The major difference is that the performance of wideband LNAs need to meet the design specifications across a relative large bandwidth. These key characteristics include

- Input Matching
- Noise Figure
- Gain
- linearity

The objective of this section is to provide the basic theory of LNA design for discussions in the following chapters.

2.1. Input Matching

Since LNA is after the antenna and band-pass filter, in order to obtain maximum power delivery, conjugate matching is needed between the output impedance of former stage and input impedance of LNA, which is typically defined to be 50-Ohm. Normally, some passive matching network always be added to the circuit to achieve good wideband or narrow band input matching in the frequency of interested, as shown in Figure 11.

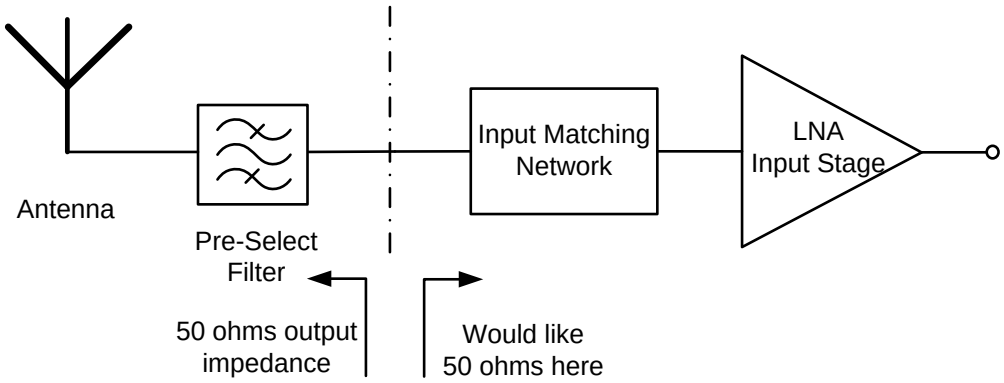


Figure 11 Input matching of LNA

The input matching of a LNA is normally characterized by its S_{11}, which is defined as

$$S_{11}=20\log\frac{\text{Reflected voltage}}{\text{Incident voltage}} \tag{2.1}$$

2.2. Noise Performance of Amplifier

2.2.1. Types of Electronic Noise

In electronic systems, noise is generated from the random fluctuation in current flows. Typically, the electronic noise can be modeled as three types of noise sources: thermal noise, short current noise and flicker noise.

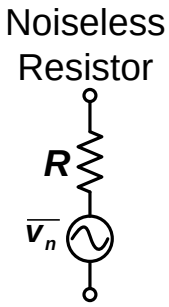


Figure 12 Noise model of a resistor

The thermal noise in resistors is generated from the random thermal motion of the carrier charges. It can be simplified as a noise voltage source

$$\overline{v_n} = \sqrt{4kTR\Delta f} \tag{2.2}$$

where T is the absolute temperature of the resistor in Kelvin, k is the Boltzmann constant ($k = 1.38\times10^{-23}\ J/K$), R is the value of the resistor and Δf is the bandwidth. Thus, the noisy resistor can be represented by a noiseless resistor series with a noise voltage source as shown in figure 12.

The power spectral density $S_v(f)$ of thermal noise can be derived as

$$S_v(f) = \overline{v_n^2} = 4kTR\Delta f \tag{2.3}$$

which is constant with respect to frequency and proportional to the absolute temperature of the component. Thurs, thermal noise is known as white noise.

Another noise mechanism is known as shot current noise. It originated from random variations of a DC current, and is always related with direct-current flow in diodes, MOS and bipolar transistors. The power spectrum density $S_i(f)$ has

$$S_i(f) = \overline{i_n^2} = 2qI_{DC}\Delta f \tag{2.4}$$

where $\overline{i_n}$ is the rms noise current, q is the electronic charge (1.6×10^{-19} Coulomb), I_{DC} is the DC current and Δf is the bandwidth. From eq. (2.4), the noise-current spectral density is constant with respect to frequency and temperature independent. Like thermal noise. Ideally, shot noise is white noise.

Flicker noise, also known as 1/f noise, is mainly caused by random capture and release of the carries at the traps near Si/SiO2 interface. Different from thermal noise

and shot noise, flicker noise is technology and frequency dependent. The spectral density of flicker noise can be modeled as

$$S_i(f) = \overline{i_n^2} = K\frac{I^a}{f^b}\cdot\Delta f \tag{2.5}$$

where K is a constant associated with process. a is a constant in the range 0.5 to 2. And b is a constant of about unity. Thus, flicker noise is considered to be inversely proportional to frequency.

Since flicker noise only concentrates at low frequencies. "Corner frequency" (f_c) is defined as the frequency at which the flicker noise density equals the white noise density. In most recent technologies, corner frequency is usually in the order of 10 MHz. Thus, flicker noise is negligible in radio frequency circuit design like low noise amplifier, while it becomes non-negligible in "baseband" applications. In this thesis, the MMW wideband LNA's operating frequency is much higher than the f_c of flicker noise. So flicker noise will not be included in the later analysis.

2.2.2. Noise in Bipolar Transistors

The small-signal equivalent circuit of a bipolar transistor including noise sources in shown in figure 13.

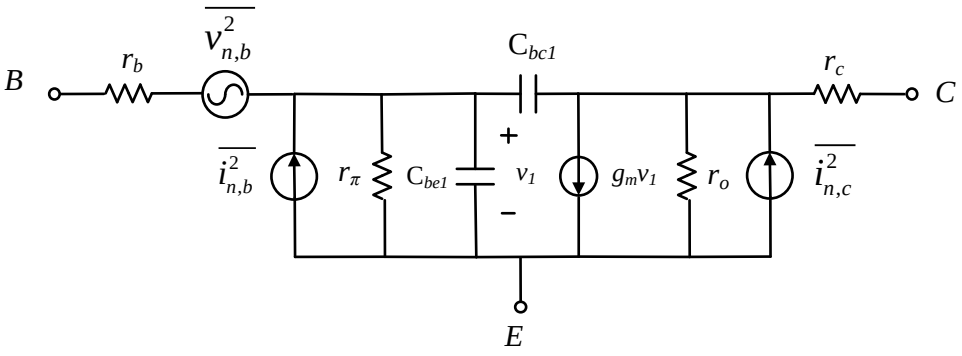


Figure 13 Bipolar small-signal model with noise sources

Three independent noise sources with mean-square values is given as:

$$\overline{v_b^2} = 4kTr_b\Delta f \tag{2.6}$$

$$\overline{i_b^2} = 2qI_B\Delta f \tag{2.7}$$

$$\overline{i_c^2} = 2qI_C\Delta f \tag{2.8}$$

Thermal noise voltage source $\overline{v_b^2}$ is originated from the transistor base resistor r_b. Shot noise current source $\overline{i_b^2}$ and $\overline{i_c^2}$ is caused by base and collector DC current I_B and I_C, respectively.

2.2.3. Noise Figure

The noise performance of an RF amplifier is characterized by its noise factor (F) or noise figure (NF, in dB). It is defined as the input signal to noise ratio (SNR) divided by the output SNR.

$$F = \frac{SNR_{in}}{SNR_{out}} \tag{2.9}$$

Noise figure (NF) is the logarithm form of noise factor (F), its unit is dB

$$NF = 10\log F \tag{2.10}$$

For RF amplifiers, SNR_{in} could be calculated as

$$SNR_{in} = \frac{P_{in}}{N_s} \tag{2.11}$$

where P_{in} is the power of input signal and N_s is the noise from the source.

Similarly, SNR_{out} is

$$SNR_{out} = \frac{P_{out}}{N_{out}} = \frac{GP_{in}}{GN_S + N_{n,out}} \tag{2.12}$$

where P_{out} is the power of the output signal, N_{out} is the total noise power at the output, G is the power gain of the amplifier, $N_{n,out}$ is the noise power contributed by the amplifier at the output. Thus, the noise factor can be given as

$$F = \frac{SNR_{in}}{SNR_{out}} = \frac{GN_S + N_{n,out}}{GN_S} = 1 + \frac{N_{n,in}}{N_S} \tag{2.13}$$

where $N_{n,in}$ is the total noise power of amplifier refer to the input.

For an n-stage cascaded front-end system in figure 14, the noise figure of the system can be derived as

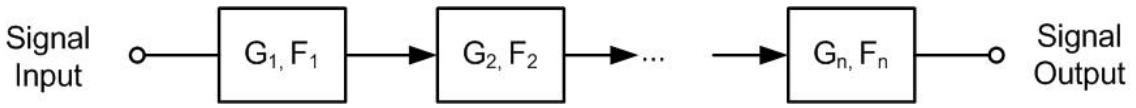


Figure 14 An n-stage cascaded front-end system

$$F = 1 + (F_1 - 1) + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} + \ldots \tag{2.14}$$

Eq. (2.14) shows that if the gain of first stage is sufficiently large, the noise figure of the system is dominated by the noise figure of the first stage.

2.3. Gain

From the noise figure perspective, LNA should provides a certain high level gain in order to reduce the noise impact from following stages to the whole system. However, this might cause tough requirement to the following stages in term of linearity, which need to be carefully addressed in budget link design.

2.4. Linearity

In reality, every amplifier is a non-linear system. The transfer function of an amplifier could be described as

$$y(t) = a_1 x(t) + a_2 x^2(t) + a_3 x^3(t) + \ldots \tag{2.15}$$

If a sinusoid $x(t) = A\cos\omega t$ is applied to the input of amplifier, Eq. (2.15) could be written as

$$y(t) = \frac{a_2 A^2}{2} + (a_1 A + \frac{3a_3 A^3}{4})\cos\omega t + \frac{a_2 A^2}{2}\cos 2\omega t + \frac{a_3 A^3}{4}\cos 3\omega t \ldots \tag{2.16}$$

In eq. (2.16), the first term on the right-hand side is a DC quantity arising from second-order nonlinearity, the second term is the "fundamental", the third and fourth are the second harmonic and third harmonic, respectively.

If $a_1 a_3 < 0$, the gain of fundamental term $(a_1 A + 3a_3 A^3/4)$ falls as *A* rises. "1-dB compression point" (P_{1dB}) is defined as the input signal level that causes the gain to drop by 1dB, as shown in figure 15. It can be calculated as

$$20\log\left|a_1 + 3a_3 A_{in,1dB}^2/4\right| = 20\log\left|a_1\right| - 1 \text{ dB} \tag{2.17}$$

It follows

$$A_{in,1dB} = \sqrt{0.145\left|\frac{a_1}{a_3}\right|} \tag{2.18}$$

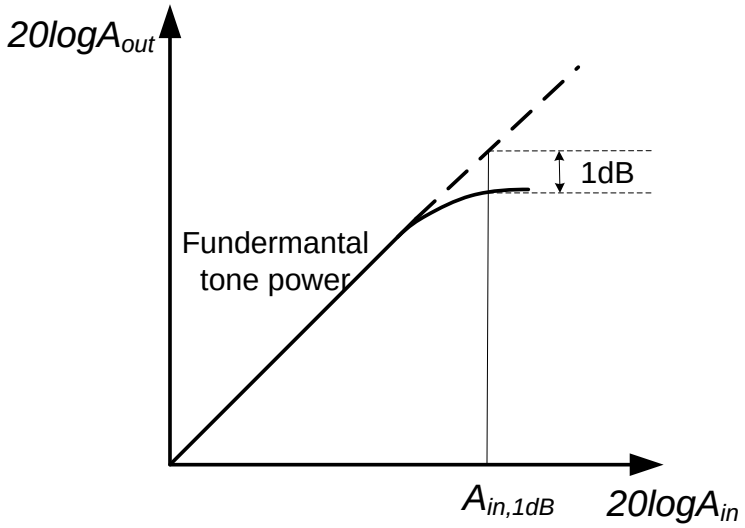


Figure 15 Definition of 1 dB compression point

If two interferers at ω_1 and ω_2 are applied to the nonlinear system. The two-tone input could be written as

$$x(t) = A_1 \cos\omega_1 t + A_2 \cos\omega_2 t \tag{2.19}$$

Then its output is

$$y(t) = a_1(A_1\cos\omega_1 t + A_2\cos\omega_2 t) + a_2(A_1\cos\omega_1 t + A_2\cos\omega_2 t)^2 + a_3(A_1\cos\omega_1 t + A_2\cos\omega_2 t)^3 \quad (2.20)$$

By expanding the right-hand side in eq. (2.20), the 3rd order inter-modulation products can be obtained as

$$\frac{3a_3A_1^2A_2}{4}\cos(2\omega_1-\omega_2)t + \frac{3a_3A_2^2A_1}{4}\cos(2\omega_2-\omega_1)t \quad (2.21)$$

These 3rd order inter-modulation products are critical to the receive front-end since they locate closely to the fundamental tone ω_1 and ω_2 in frequency spectrum, as shown in figure 16, and are difficult to be eliminated using on-chip band pass filters.

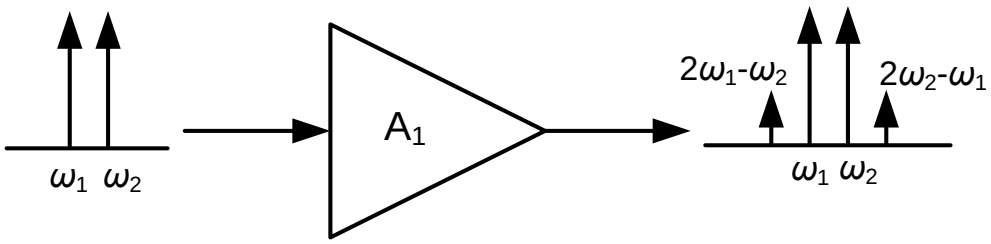


Figure 16 3rd order inter-modulation

The input referred 3rd order intercept point (IIP3) is defined as the input power level that the fundamental tone output power is equal to the 3rd order inter- modulation (IM_3) tones output power. In figure 17, by extrapolating the fundamental tone output with the slope=1 and the 3rd order inter-modulation (IM_3) tones with the slope=3 from a low input power level until they intercept each other, IIP3 can be obtained as the x-coordinate of the intersection point, and the y-coordinate is called the output referred 3rd order intercept point (OIP3).

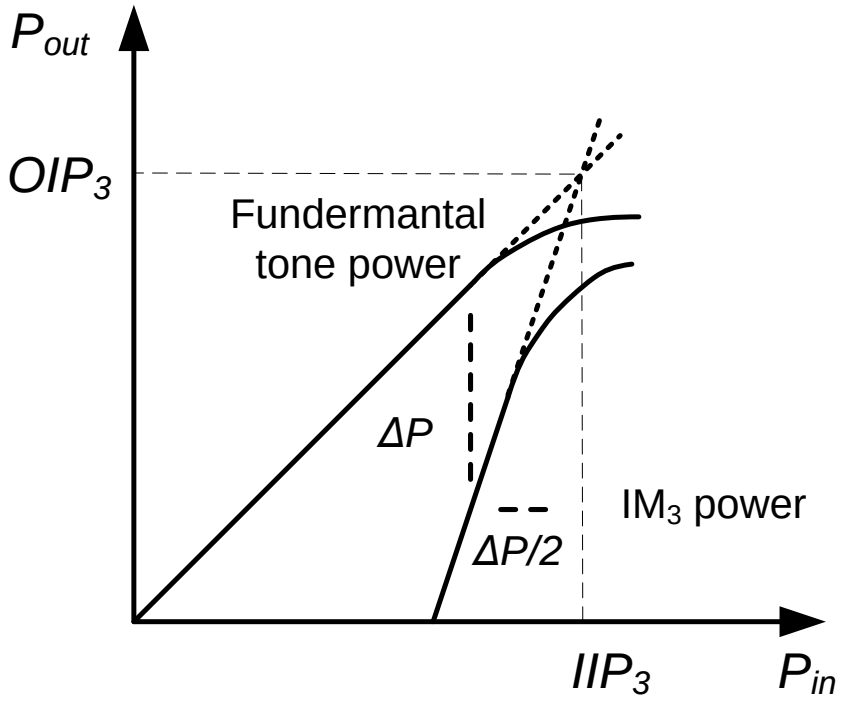


Figure 17 3rd order intercept point

Besides the characteristics we just discussed above, in LNA circuit, power consumption and chip area are also very important feature that need to be addressed since they affect the applicability and cost of wireless applications.

CHAPTER III

WIDEBAND LOW NOISE AMPLIFIER DESIGN

This chapter starts with the fundamental of feedback theory. Then the embedded positive-negative feedback theory will be introduced. Finally, a frequency-controlled positive-negative feedback wideband LNA in 0.18-μm BiCMOS process will be presented with detailed circuit analysis.

3.1. Fundamentals of Feedback Theory

An ideal feedback configuration is shown in figure 18.

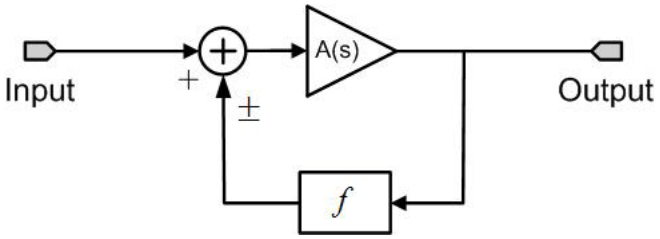


Figure 18 An ideal feedback configuration

The transfer function *H(s)* of this feedback system can be given as

$$H(s) = \frac{output\ signal}{input\ signal} = \frac{A(s)}{1 \pm fA(s)} \tag{3.1}$$

where *A(s)* is gain of feed forward amplifier. f is the feedback factor. The plus or minus sign in the denominator represent negative or positive feedback, respectively.

Since the input and output signal may be voltages or currents, there are four combinations existing. Therefore, four types of basic feedback configuration are considered.

3.1.1. Voltage-Voltage Feedback

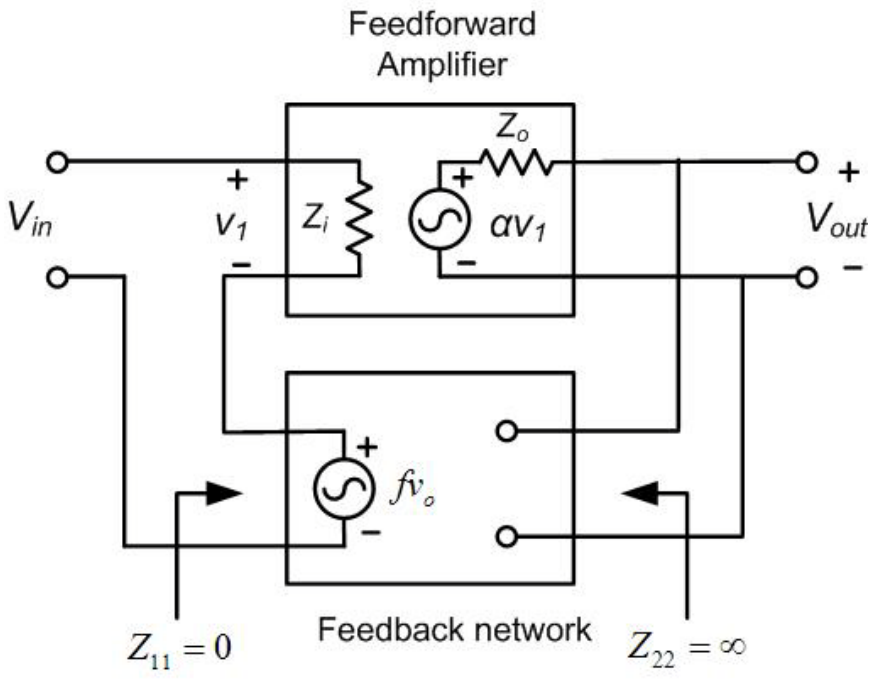


Figure 19 Voltage-Voltage feedback

Figure 19 shows a voltage-voltage feedback topology. The feedback network senses output voltage v_{out} and return a voltage signal fv_o in series with input voltage. The closed-loop voltage gain is

$$Gain_{v,v} = \frac{v_{out}}{v_{in}} = \frac{\alpha}{1+\alpha f} \tag{3.2}$$

3.1.2. Voltage-Current Feedback

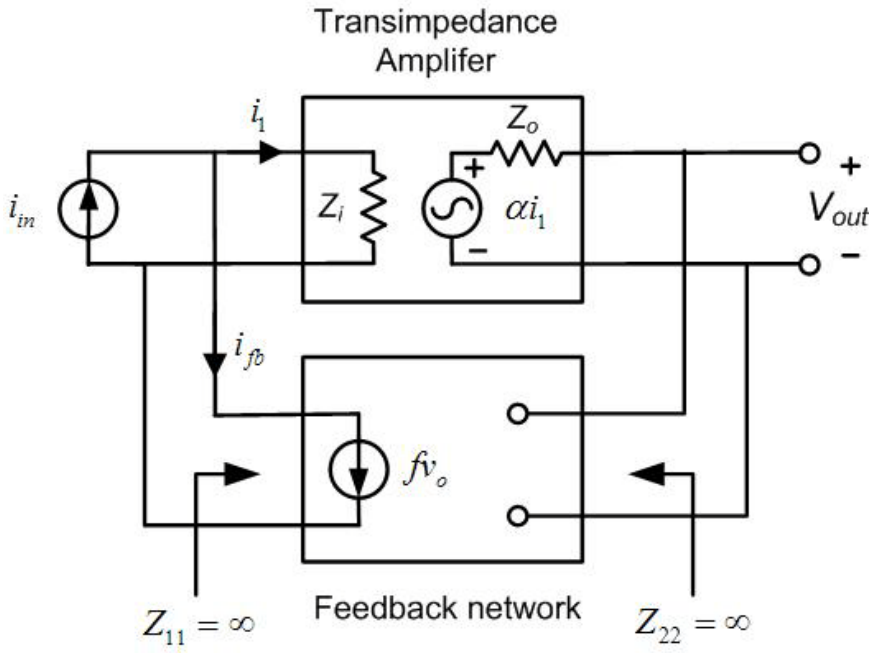


Figure 20 Voltage-Current feedback

The voltage-current feedback topology is shown in figure 20. The input current signal is transferred to output voltage v_{out} by a transimpedance amplifier, while the feedback network senses the output voltage back to input as current signal fv_o. The closed-loop gain has

$$Gain_{v,i} = \frac{v_{out}}{i_{in}} = \frac{\alpha}{1+\alpha f} \tag{3.3}$$

3.1.3. Current-Voltage Feedback

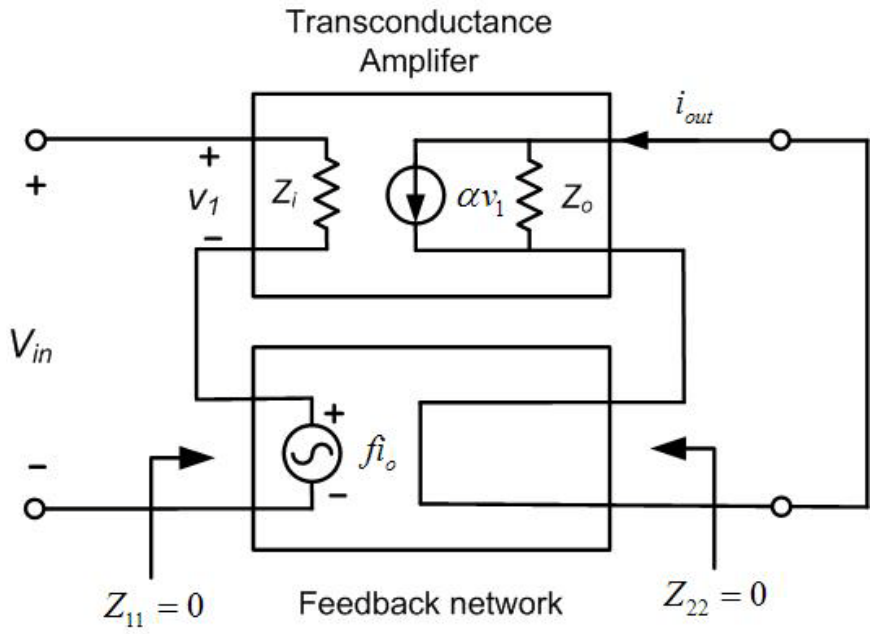


Figure 21 Current-Voltage feedback

Figure 21 shows a current-voltage feedback topology. The feedback network senses the output current i_{out} and return a voltage signal fi_o in series with input voltage. The closed-loop voltage gain is

$$Gain_{i,v} = \frac{i_{out}}{v_{in}} = \frac{\alpha}{1+\alpha f} \tag{3.4}$$

3.1.4. Current-Current Feedback

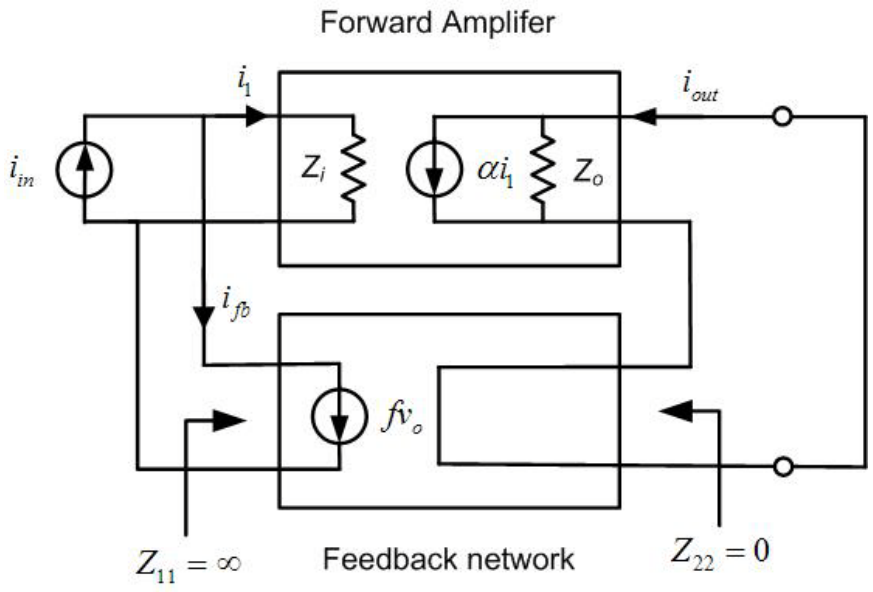


Figure 22 Current-Current feedback

Figure 22 shows a current-current feedback topology. The feedback network senses the output current i_{out} and return a current signal fi_o in shunt with input current. The closed-loop current gain is

$$Gain_{i,i} = \frac{i_{out}}{i_{in}} = \frac{\alpha}{1+\alpha f} \tag{3.5}$$

From above discussion, all four feedback configuration have same gain expression as eq. (3.1). Nowadays, Feedback circuit and system is widely used in various applications.

3.2. The Embedded Positive-Negative Feedback Technology

LNA designs utilizing positive feedback technology for gain enhancement have been reported in [8]-[9]. The positive feedback closed loop gain is given as

$$A_p(s) = \frac{A(s)}{1 - f_P A(s)} \tag{3.6}$$

As the denominator $0 < 1 - f_P A(s) < 1$, the close loop gain $A_P(s) > A(s)$, and gain boosting can be achieved. However, the positive feedback amplifier is sensitive to the process and environment variations. In the case $f_P A(s)$ close to 1, $A_P(s)$ will increase significantly or even cause the amplifier to oscillate. In order to enhance the stability of the circuit, a negative feedback configuration with embedded positive feedback stage is discussed in [10]. As shown in figure 23, the inner positive feedback stage provides gain enhancement while the outer negative feedback improves the stability, desensitizing the whole system gain to process and environmental variations. The transfer function is given as

$$A_{P-N}(s) = \frac{A_P(s)}{1 + f_N A_P(s)} = \frac{A(s)}{1 - f_P A(s) + f_N A(s)} \tag{3.7}$$

In eq. (3.7), the negative feedback loop introduces an additional term $f_N A(s)$ in the denominator comparing to eq. (3.6). In the undesired case that $1 - f_P A(s) \approx 0$, this term assures the stability of the system, and the whole system gain is approximated to $1/f_N$.

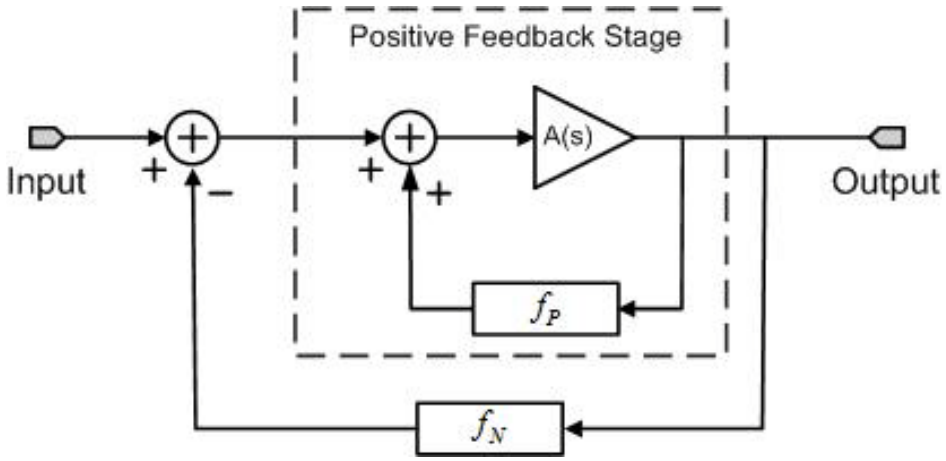


Figure 23 The embedded positive-negative feedback configuration

In [10], the theoretical analysis of the embedded P-N feedback using first-order model is described. However, circuit implementation using this theory has not been seen in literatures. In this thesis, the first ultra-wideband LNA topology utilizing P-N feedback along with the analysis and measurement result is presented in the following sections.

3.3. The Proposed Ultra-Wideband LNA Topology

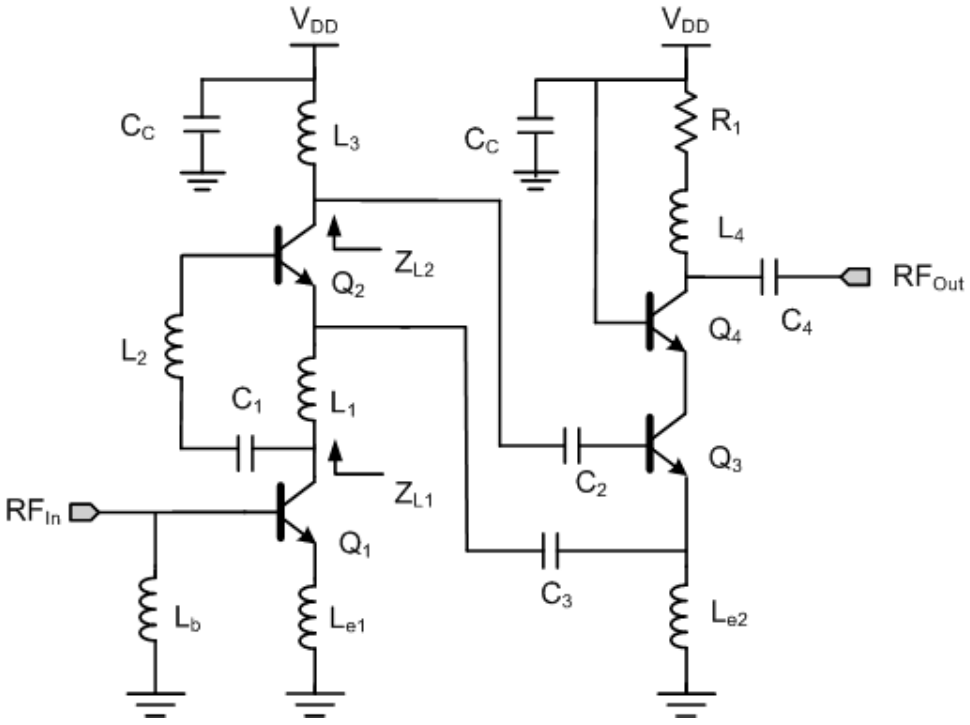


Figure 24 Schematic of proposed ultra-wideband LNA
(Biasing circuit is not shown).

The schematic of the proposed ultra-wideband LNA is shown in Figure 24, where the Q_1 and Q_2 stages adopt a current-reused cascaded structure. The load impedances, Z_{L1} and Z_{L2} are designed to achieve maximum impedance at the lower-band (20 GHz) and upper-band (60 GHz) frequency, respectively. The emitter current of Q_3 has two feedback paths through the bypass capacitor C_3. One is connected to the emitter of Q_2, forming a positive feedback loop. Another path is connected to the base of Q_2 through the inter-stage network L_1, L_2, and C_1, forming a negative feedback path.

Therefore, an embedded P-N current feedback is realized. At the output of the amplifier, a shunt-peaking load stage of L_4 and R_1 is utilized to achieve wideband output matching.

3.3.1. Wideband Input Matching

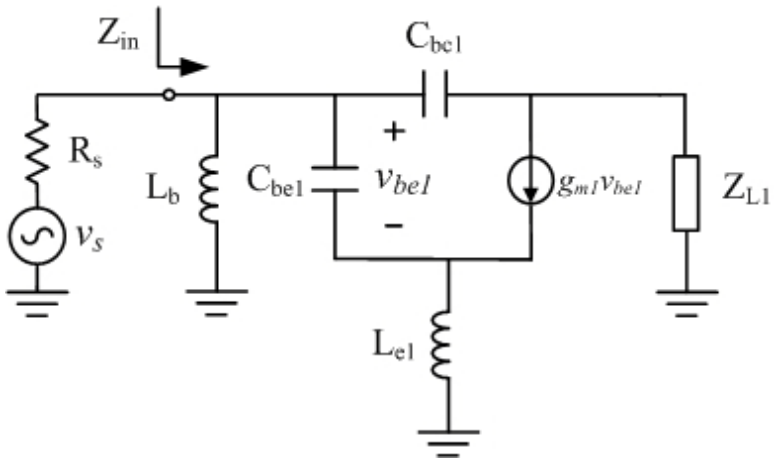
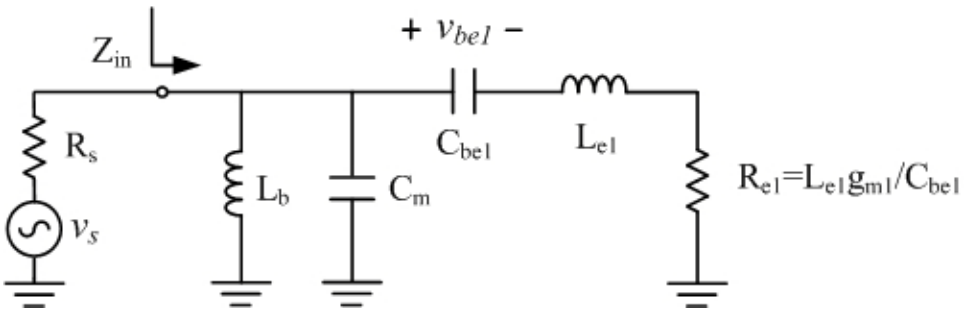


Figure 25 Small-signal equivalent circuit model of the input matching network (neglecting r_b, r_π and r_o).



(b)

Figure 26 Equivalent four-order doubly terminated band-pass filter of the input matching network

Figure 25 shows the small-signal equivalent circuit model of the wideband input matching network, which consists of the inductors L_b, L_{e1}, transistor Q_1 and load impedance Z_{L1}. The input impedance Z_{in} can be given as follows:

$$Z_{in}(s) \approx \frac{sL_b(1+sL_{e1}g_{m1}+s^2L_{e1}C_{be1})}{1+sL_{e1}g_{m1}+s^2(L_bC_m+L_bC_{be1}+L_{e1}C_{be1})+s^3L_{e1}L_bg_{m1}C_m+s^4L_{e1}L_bC_{be1}C_m} \tag{3.8}$$

with

$$C_m = C_{bc1}\left[1-\frac{Z_{TL1}}{1+sC_{bc1}Z_{TL1}}(sC_{bc1}-g_{m1}\frac{1}{1+g_{m1}sL_s+s^2L_{e1}C_{be1}})\right] \tag{3.9}$$

C_m represents the miller reflected capacitance.

Eq. (3.8) can be rearranged and simplified as

$$Z_{in}(s) \approx sL_b \,\|\, \frac{1}{sC_m} \,\|\, [sL_{e1}(1+\frac{g_{m1}}{sC_{be1}})+\frac{1}{sC_{be1}}] \tag{3.10}$$

By selecting the size and biasing of Q_1 as well as inductance of L_{e1}, equivalent impedance $R_e = L_{e1}g_{m1}/C_{be1}$ can be set to equal to R_s with frequency independence. The wideband input matching network can be regarded as a four-order doubly terminated band-pass filter as shown in Figure 26.

Figure 27 shows the simulated input return loss of the proposed LNA. Without shunt inductor L_b, C_{be1} and L_{e1} resonate at the mid-band of interest, and the input matching network shows a narrow band characteristic. L_b introduces a parallel resonance with the C_{be1} and L_{e1} series circuit, shifting the resonance frequency to lower band. In addition, L_b and C_m parallel circuit with the C_{be1} and L_{e1} series circuit shows another

resonance at the upper band frequency. The overall wideband input matching characteristic is therefore achieved.

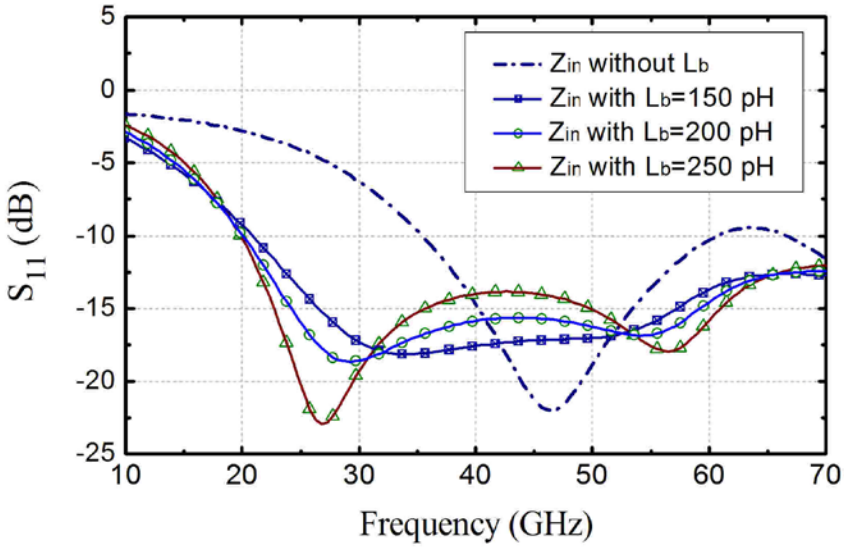


Figure 27 Input return loss with/without various values of L_b.

3.3.2. Frequency Response of S21

The proposed frequency-controlled P-N feedback topology is shown in Figure 28, where L_{e2}, C_3 and L_1 compose the embedded positive current-voltage and negative current-current feedback network. Applying the basic feedback theory and neglecting the feed-forward effect and the bypass capacitor C_3, the equivalent circuit to Figure 28 using two-port representation of the feedback network is shown in Figure 29.

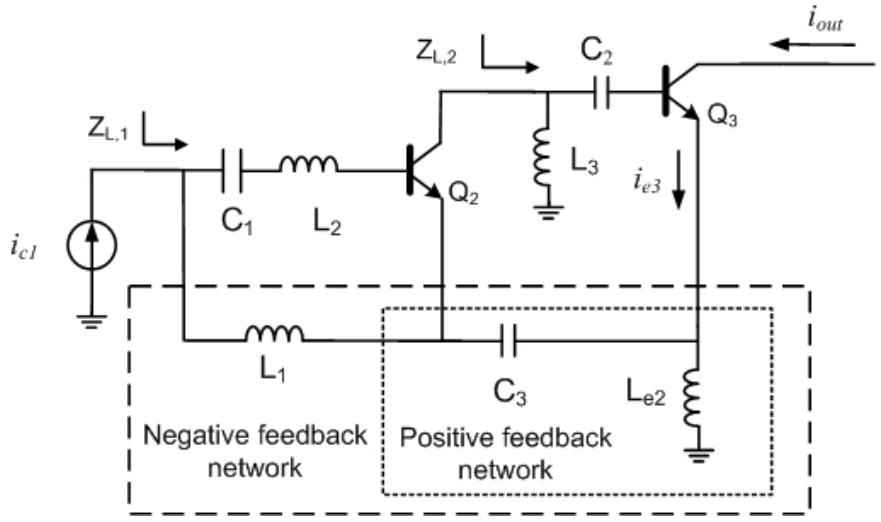
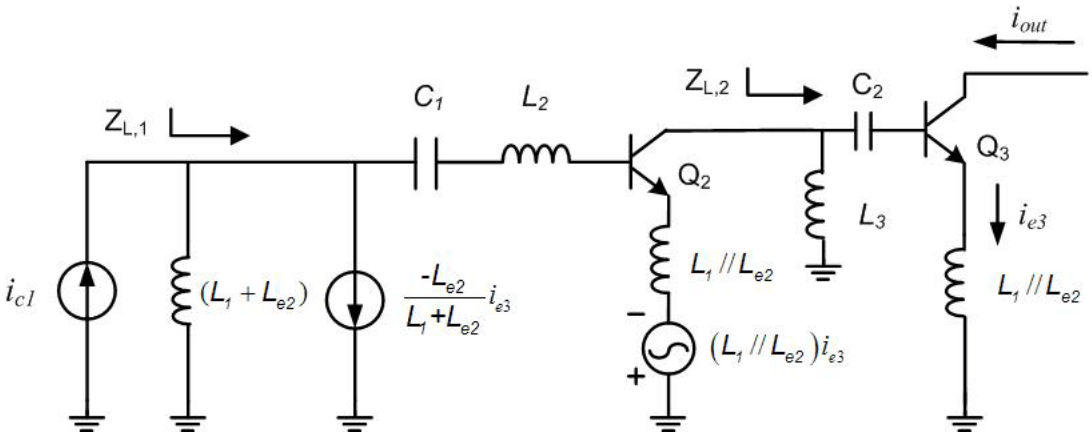


Figure 28 The topology of embedded positive-negative current feedback.



(b)

Figure 29 A two-port representation of the feedback network.

In figure 29, current source i_N and voltage source v_P is utilized to represent the negative and positive feedback effect, respectively. Assuming the ratio of emitter to collector current $\alpha \approx 1$, current source i_N is

$$i_N = (\frac{-L_e}{L_1 + L_e}) i_{e3} \tag{3.11}$$

which is frequency independent and constant proportional to emitter current of Q_3, i_{e3}.

The voltage source v_P is

$$v_P = j\omega(L_1 // L_{e2})i_{e3} \tag{3.12}$$

which is proportional to i_{e3} as well as frequency. Therefore, as operating frequency increases, positive feedback will become more and more significant.

Applying the small–signal model of transistor into figure 29, the resonant frequency of Z_{L1} can be derived as

$$\omega_L = \sqrt{\frac{C_1 + C_{be2}}{(L_1 + L_{e2} + L_2 + L_1 \| L_{e2})C_1 C_{be2}}} \tag{3.13}$$

C_{be2} is the base-emitter capacitor of Q_2.

The quality factor of Z_{L1} is

$$Q_L = \frac{1}{r_{b2} + g_{m2}\dfrac{(L_1 \| L_{e2})}{C_{be2}}} \sqrt{\frac{(L_1 + L_{e2} + L_2 + L_1 \| L_{e2})(C_1 + C_{be2})}{C_1 C_{be2}}} \tag{3.14}$$

r_{b2} and g_{m2} is base resistance and transconductance of Q_2, respectively.

To investigate the effect of frequency-controlled P-N feedback to the LNA's S_{21}, Figure 30 plots the simulated S_{21} versus frequency under the conditions g_{m1}= g_{m2}= 150 mS, g_{m3}=220 mS, L_{b1} = 250 pH, L_1=200 pH, L_2= 40 pH , L_3= 80 pH, L_4 = 100 pH, L_{e1}= 45 pH, C_1= 140 fF,C_2= 100 fF, C_3 = 2 pF, C_1 = 1 pF, R_1 = 40 Ω while sweeping L_{e2} from 0 to 400 pH in the step of 100 pH. When L_{e2}= 0, the feedback loop does not exist. The circuit becomes a typical current reused configuration following by a CE of Q_3 stage. The lower-band resonant frequency ω_L is around 30 GHz. And the upper-band gain roll-

off is significant. As L_{e2} increases, the P-N feedback effect starts taking into account. At the upper-band frequency, the gain boosting effect appears due to the dominated positive feedback. As L_{e2} rises, the upper-band gain increases. Meanwhile the resonant frequency of lower-band is shifted to the lower frequency, as predicted in eq. (3.13). And the peak gain at the lower-band is reduced due to the negative feedback. Therefore, the overall bandwidth of the LNA is widened. To verify the effect of negative feedback on moderating the process of upper-band gain boosting, figure 31 shows the simulation of S_{21} with fixed L_{e2} of 300 pH and sweeping L_1 from 100 to 300 pH. As L_1 increases, with stronger gain suppression from the negative feedback, the process of upper-band gain boosting becomes milder, desensitizing the undesirable effect of process and environmental variations.

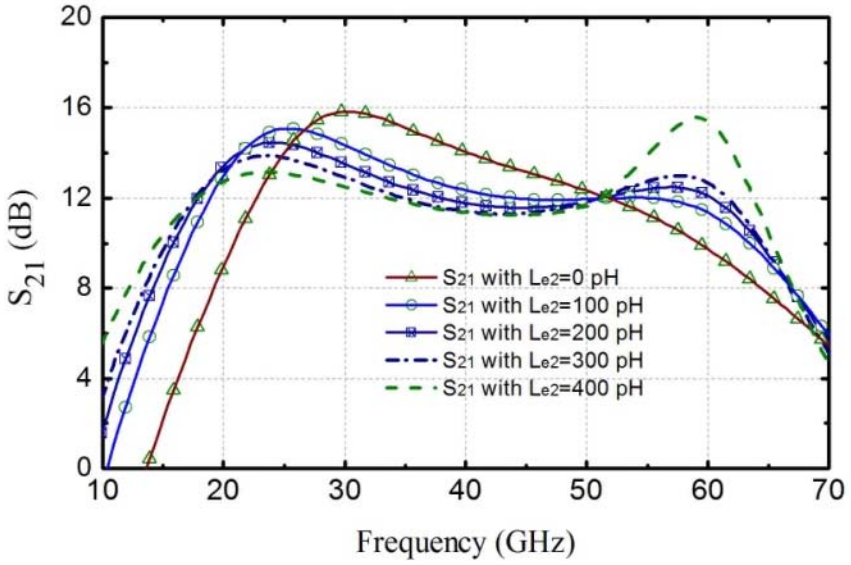


Figure 30 Simulated S_{21} versus frequency of the proposed wideband LNA with various values of L_{e2}

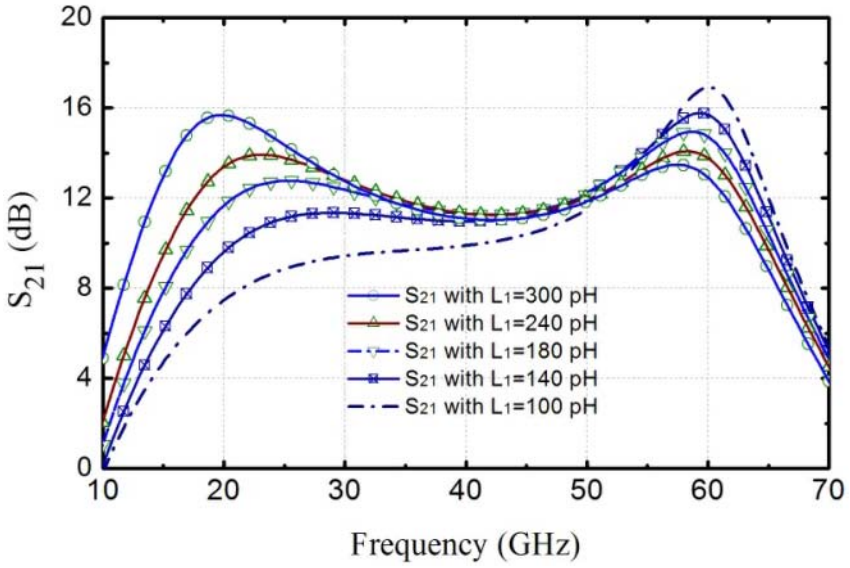


Figure 31 Simulated S_{21} versus frequency of the proposed wideband LNA with various values of L_1.

From discussion above, the positive and negative feedbacks have dominated effect at the upper-band and lower- band, respectively. By properly selecting the value of L_1 and L_{e2}, one can adjust the gain response of the amplifier across the full-band to improve the gain flatness.

3.3.3. Noise Analysis

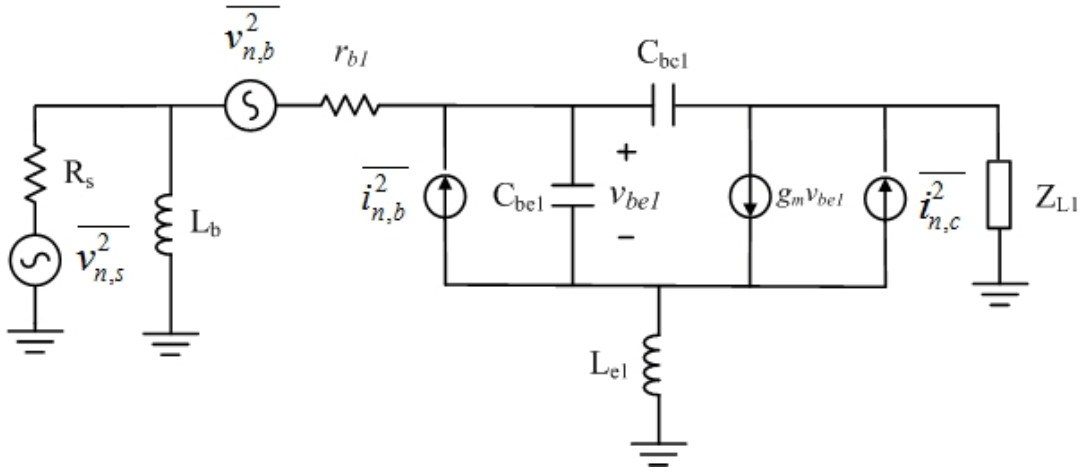


Figure 32 Small-signal equivalent circuit of Q_1 stage with noise source.

The noise figure of proposed LNA is mainly affected by the input Q_1 stage, which is shows in figure 32 using small-signal equivalent circuit and including the thermal noise source $\overline{v_{n,b}^2}$ of base resistance r_{b1}, and shot noise sources of base and collector current $\overline{i_{n,b}^2}$, $\overline{i_{n,c}^2}$. The noise figure is given as

$$NF \approx 1+\frac{r_{b1}}{R_s}\left(1+\frac{R_s}{\omega^2 L_b^2}\right)+\frac{g_{m1}}{2\beta R_s}\left|(R_s+r_{b1})+\frac{R_s R_{b1}}{sL_b}+sL_{e1}+\frac{L_{e1}R_s}{L_b}\right|^2 + \frac{1}{2g_{m1}R_s}\left|1+sC_{M1}(R_s+r_{b1})+\frac{R_s}{sL_b}+\frac{R_s(r_{b1}+sL_{e1})C_{M1}}{L_b}\right|^2 \quad (3.15)$$

where $C_{M1}=C_{be1}+C_{bc1}$.

To improve the NF, L_b should have large inductance value. The base resistance r_{b1} can be reduced by increasing the base area of Q_1 and using multi-emitter fingers. However, this will also increase C_{bc1} and C_{be1}, shifting the passband of input matching

network to lower frequency, which need to be carefully adjusted. In eq. (3.15), the noise contribution of $\overline{i_{n,b}^2}$, $\overline{i_{n,c}^2}$ are proportional and inversely proportional to g_{m1}, respectively. Therefore, an optimum g_{m1} can be found to achieve the minimum NF [11], with

$$g_{m1,opt} \approx \sqrt{\beta}\left|\frac{R_s + sL_b + sR_s(r_{b1} + sL_{e1})C_{M1} + s^2L_b(R_s + r_{b1})C_{M1} + s^3L_bL_{e1}C_{M1}}{r_{b1}R_s + (r_{b1} + R_s)sL_b + sL_{e1}R_s + s^2L_bL_{e1}}\right| \tag{3.16}$$

where β is the current gain of BJT.

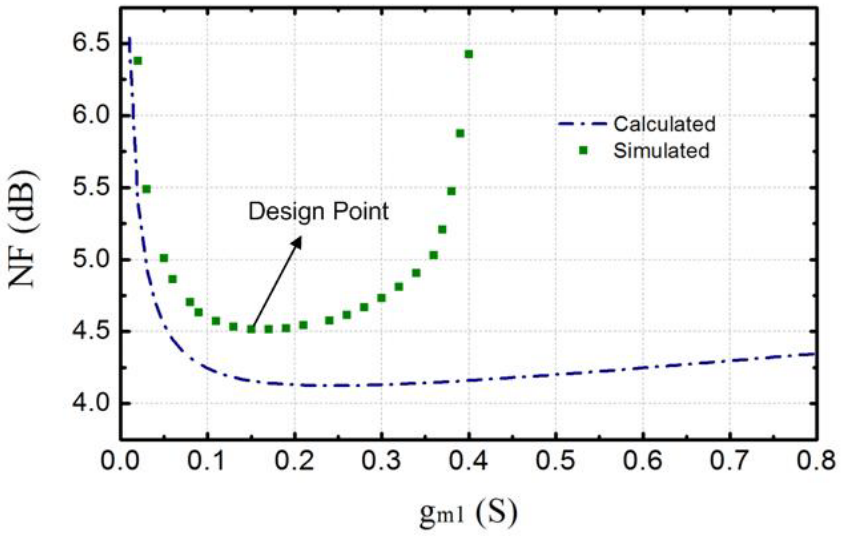


Figure 33 The calculated and simulated NF versus g_{m1}.

Figure 33 shows the plot of NF sweeping with g_{m1} at 40GHz. By fixing other component values in eq. (3.16), the minimum NF can be achieved at g_{m1}=0.25 S. The noise contribution of current $\overline{i_{n,b}^2}$, and $\overline{i_{n,c}^2}$ becomes the dominated factor to the overall noise at the range below and above the $g_{m,opt}$, respectively. In practice, since C_{bc1} and C_{be1} increase with g_{m1}, the noise of I_{C1} term increases much faster above $g_{m1,opt}$, and

worsens the overall NF, as the simulation result shown. In this design, the g_{m1}= 0.15 S is selected as the design point.

3.4. WB LNA Implementation

The proposed wideband LNA was designed and fabricated using Jazz 0.18-μm BiCMOS process ($f_T \approx$ 200 GHz) [12]. The transistor sizes and the value of passive components are determined based on the circuit analysis above and optimized using Cadence [13].

In MMW integrated circuits, the poor quality factor of on chip inductors and parasitic of inter-connection line have non-neglectable effect on circuit performance, limiting the operation bandwidth of the LNA and degrading the gain at the upper-end of desired band. In this design, inductors are implemented using the top and thickest metal layer (Metal 6 with 2.81μm thickness) to minimize the resistive loss (with quality factor Q > 14) and ensure the self-resonant frequencies are far away (>120 GHz) from the desired frequency band. In addition, the inter-connection lines are realized using multiple layers stacked if needed. The full-wave electromagnetic simulator HyperLynx 3D EM is used to model all the passive signal paths in this LNA design [14]. Table 1 lists the parameters of the designed WB LNA. Considering the trade-off between gain, NF and power consumption, the current-reused transistors Q_1 and Q_2 is sized with an emitter area of 0.15× 7μm^2 and biased at a dc current of 4.4 mA. The transistor Q_3 and Q_4 have emitter area of 0.15× 8um^2 with 4.8 mA dc current. The DC supply voltage is

1.8V. The die microphotograph of the WB LNA is shown in Figure 34, with a chip area of 700×400 μm^2, excluding pads.

Table 1 WB LNA's Parameters

Circuit Elements and Value			
Q_1, Q_2	0.15μm x 7μm emitter area		
Q_3, Q_4	0.15μm x 10μm emitter area		
C_1	160 fF	C_2	100 fF
C_3	2 pF	C_4	400 fF
L_1	200 pH	L_2	40 pH
L_3	80 pH	L_4	100 pH
L_{e1}	45 pH	L_{e2}	300 pH
L_b	250 pH	R_1	40 Ω

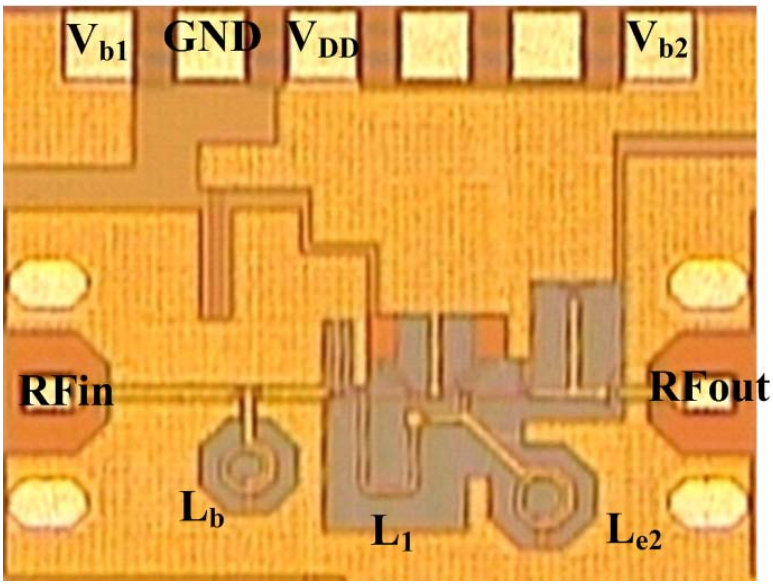


Figure 34 Die microphotograph of the proposed WB LNA.

3.5. Measurement Results

The proposed wideband LNA is measured on-chip using the Rohde & Schwarz ZVA67 vector network analyzer (VNA). The RF input, output signals are applied using the Cascade Microtech's DC-67 GHz Infinity G-S-G probe and the DC biasing are supplied using 6 pins DC probe to minimize possible mismatch and loss from the measurement setup. The Short-Open-Load-Thru calibration method along with Cascade Microtech's impedance standard substrate standards is used for calibration from 10 GHz to 67 GHz.

In the noise figure measurement, the measurement process is divided to two parts. For the frequency range below 24 GHz, the noise figure of LNA can be measured directly with the VNA, as shown in figure 35. For the frequency range above 24 GHz, the VNA will first down-convert the RF input signal from the LNA output to low frequency using a internal mixer, then perform the noise figure measurement. Therefore, the original low frequency noise may overlap with the down-converted signal and cause inaccurate result. To avoid this measurement deviation, a high pass filter (HPF) with 24 GHz cutoff frequency is needed after the LNA in order to block the low frequency interference. Sometimes, an additional pre-amplifier is also need to provide sufficient gain to restrain the noise from the internal mixer, as shown in figure 36.

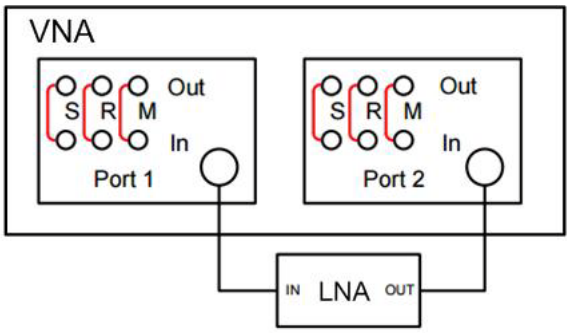


Figure 35 VNA noise figure measurement basic configuration

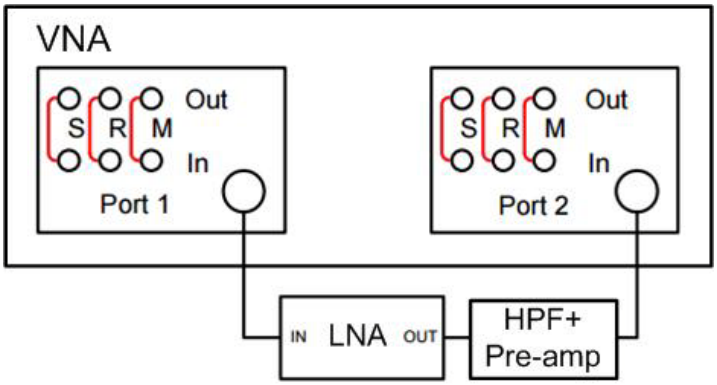


Figure 36 VNA noise figure measurement with HPF and pre-amp.

Figure 37 and 38 shows the simulated and measured S-Parameters the LNA. In Figure 37, the amplifier exhibits a measured power gain (S_{21}) of 10.5 dB with ±0.5 dB ripple from 20 to 57 GHz. The measured input return loss (S_{11}) is better than 10dB across the entire band of interest. In Figure 38, the output return loss (S_{22}) is better than 15 dB. It is noted that the measured reverse isolation (S_{12}) of the amplifier degrades with the increasing of frequency, which is mainly due to the coupling effect of the parasitic capacitor from the inter-connection and substrate. However, an isolation of 30 dB can still be achieved at 58 GHz.

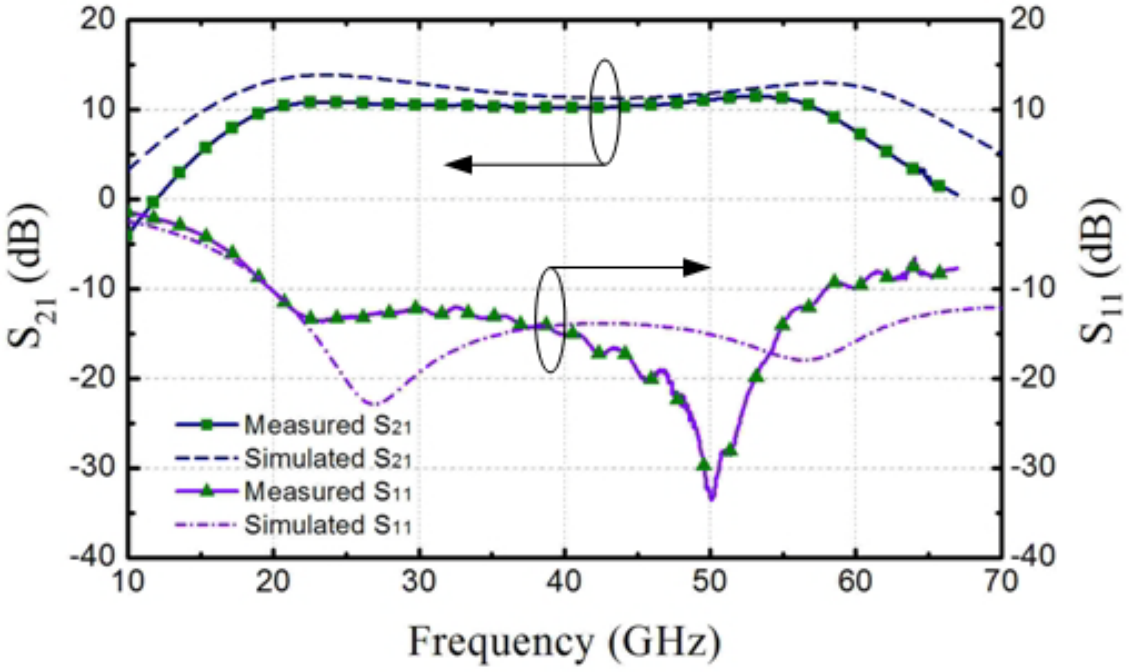


Figure 37 Measured and simulated S_{21} &S_{11} versus frequency

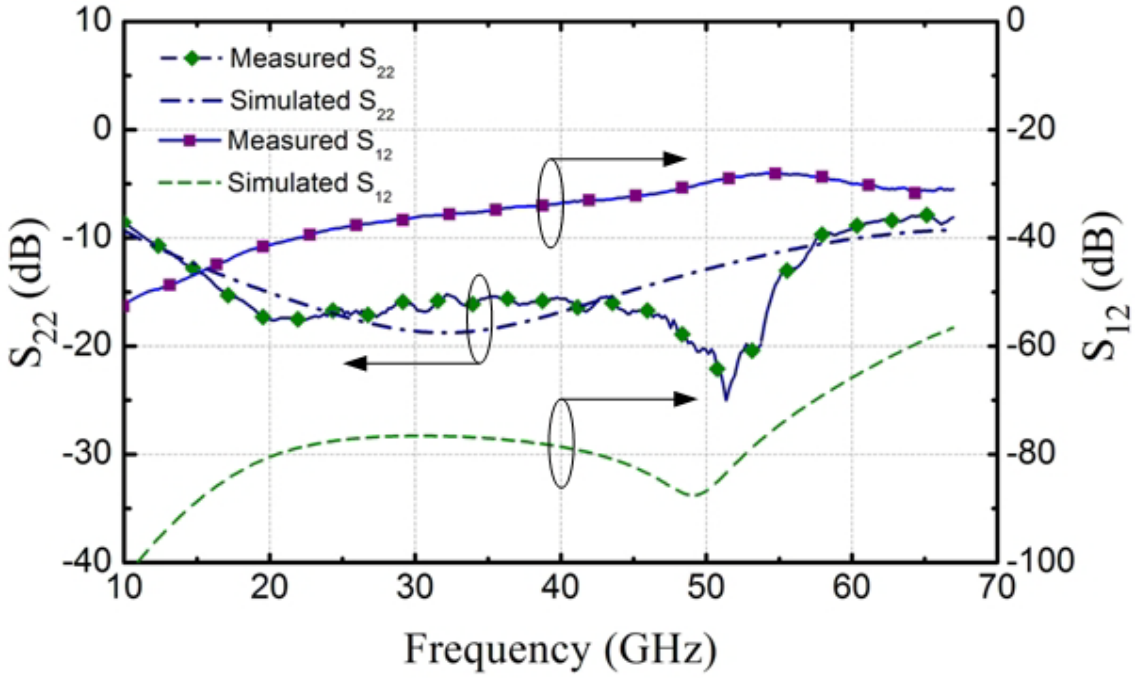


Figure 38 Measured and simulated S_{22}& S_{12} versus frequency

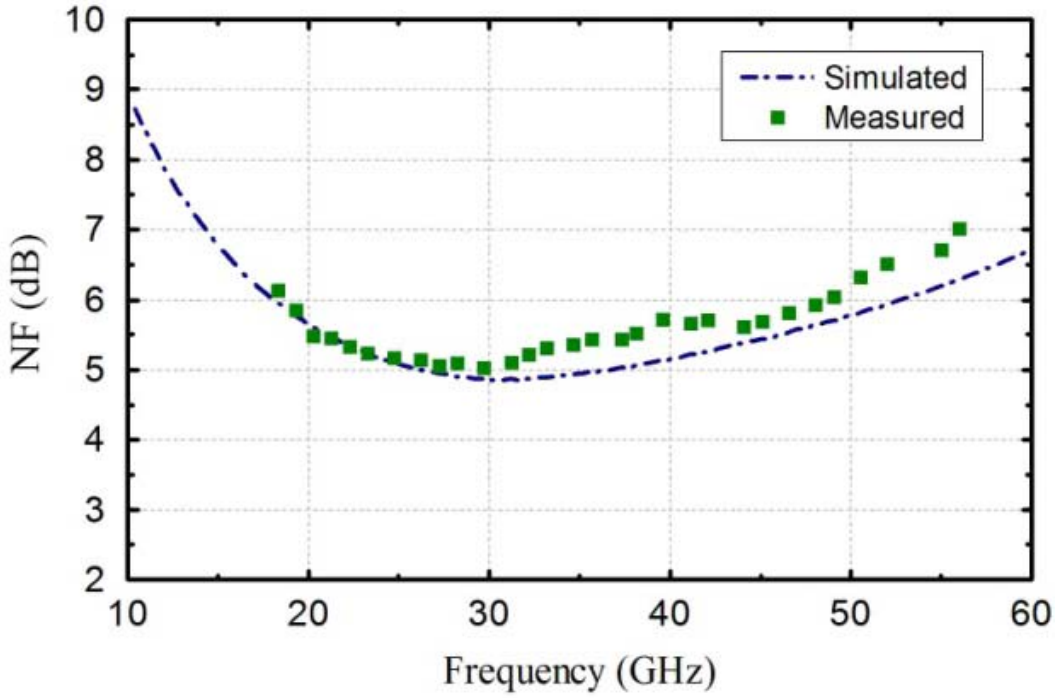


Figure 39 Measured and simulated NF versus frequency.

Figure 39 shows the simulated and measured noise figure of the LNA. The minimum NF of 5.1 dB is achieved at around 27 to 30 GHz range. At 56 GHz, the maximum NF is 7 dB.

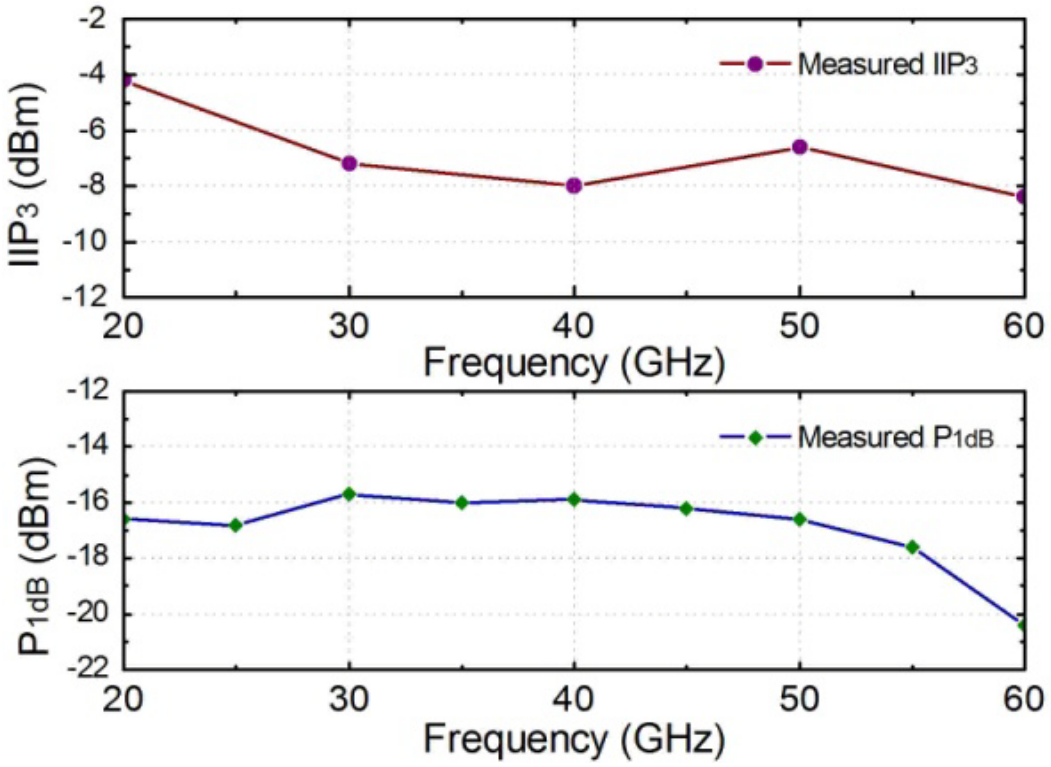


Figure 40 Measured and simulated P1dB and IIP3 versus frequency.

Linearity test is performed in discrete frequency points and presented in Figure 40. The input 1 dB compression point (P1dB) is from -16 to -19 dBm. Two tone testing using signals with the same amplitude and 1 MHz offset is applied. The measured input intercept point (IIP3) is above -8 dBm in the whole band.

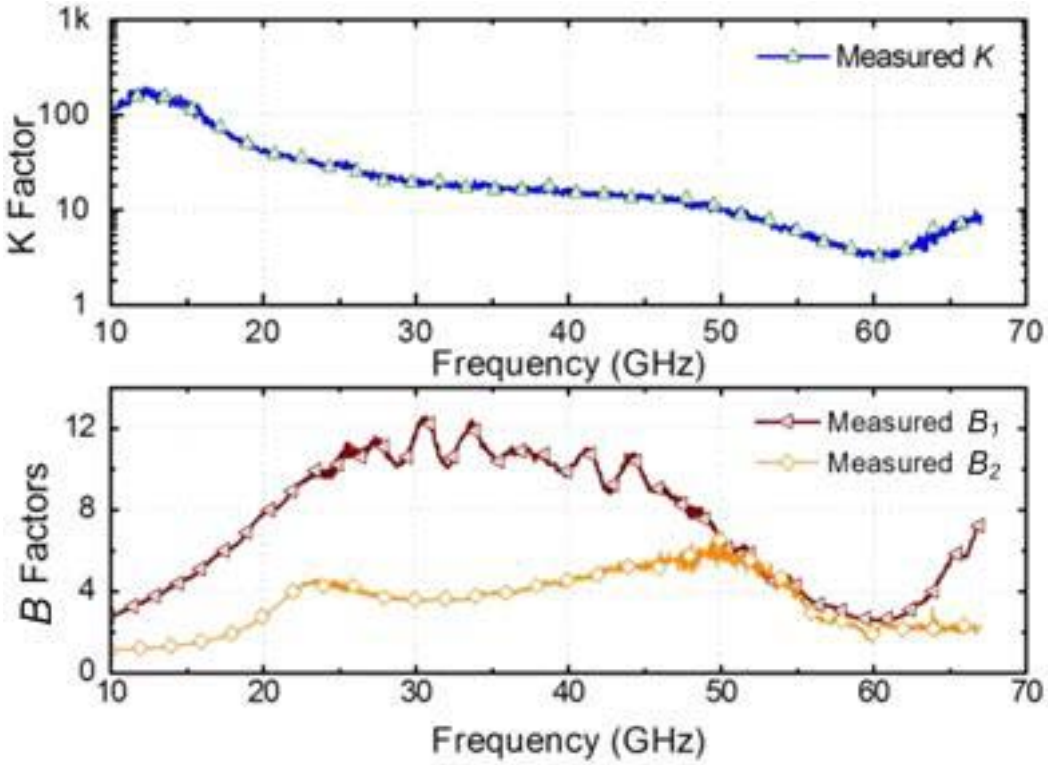


Figure 41 Measured stability factor *K* and *B* versus frequency.

To confirm the unconditional stable of the LNA circuit, the stability factors *K* and *B* are measured and shown in figure 41, which shows $K > 1$ and $B > 0$ across the whole band.

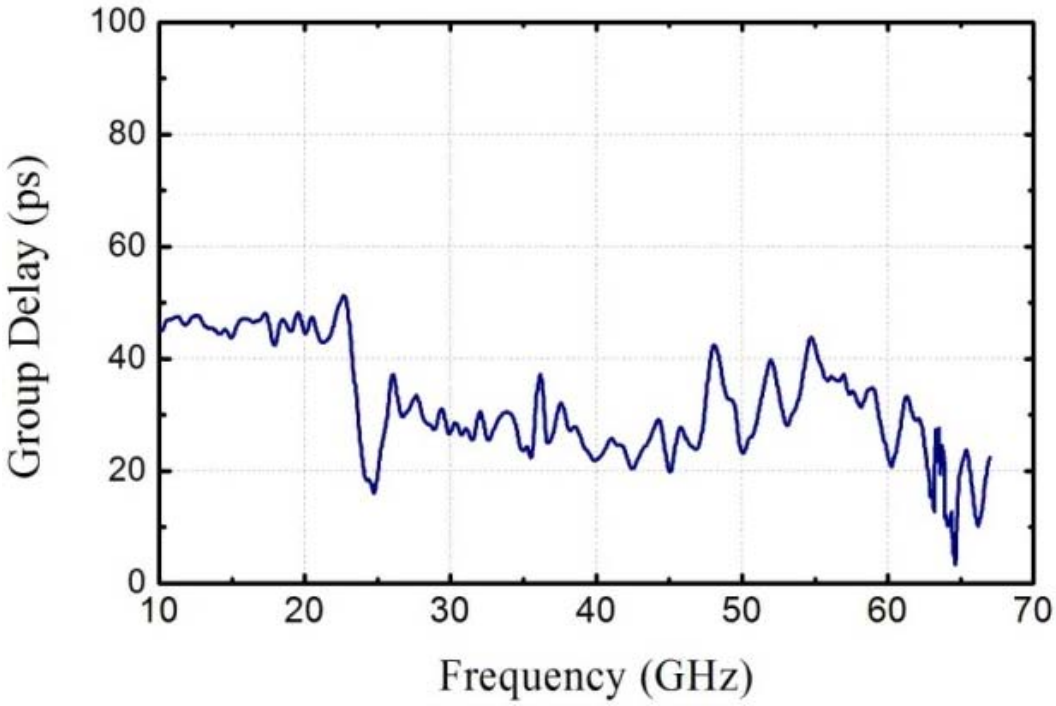


Figure 42 Measured group delay versus frequency.

Figure 42 shows the measured group delay. The in-band average delay is about 30 ps with maximum and minimum values of 51 ps and 16 ps, which shows a good phase linearity property.

Table 2 Summary of the Proposed Mmw Wideband LNA
Performance, and Comparison With Previously Published Designs

Ref.	Freq. Range (GHz)	BW (GHz)	Peak Gain (dB)	S11 (dB)	NF (dB)	Input P_{1dB} (dBm)	P_{DC}(mW) /V_{DD}	f_T (GHz)	F.O.M	Tech.
[2] JSSC/2004	26 - 42	16	11.9	-6	3.6 - 4.1[a]	N/A	40.8/2.4V	149	0.74	90 nm SOI CMOS
[3] MTT/2009	47.7 - 61.3	13.6	16	< -5.5	4.5 - 8.4[b]	N/A	10/2V	N/A	N/A	65 nm CMOS
[5] Q-Band LNA MTT/2012	29 - 44	15	13.8	< -12	3.8 - 6.4[c]	-10 @ 37GHz	18/1.2V	N/A	N/A	90 nm CMOS
[5] V-Band LNA MTT/2012	46 -63	17	17	< -10	4.4 - 7.7[c]	-16 @ 60GHz	19.2/1.2V	N/A	N/A	90 nm CMOS
[15] SiRF/2008	54 - 70	16	15.8	< -8	6.9 - 8[d]	N/A	24/2.5V	200	0.6	0.18 μm BiCMOS
This work	20 - 57	37	11	< -10	5.1- 7	-17.8 @ 55 GHz	16.6/1.8V	200	1.56	0.18 μm BiCMOS

a. Estimated from the measured response in Fig. 12 of [2]
b. Estimated up to 61GHz from the measured response in Fig. 22 of [3]
c. Estimated from the measured response in Fig. 21 & Fig. 23 of [5]
d. Estimated from the measured response in Fig. 4 of [15]

Finally, the performance of the proposed wideband LNA along with recently published MMW wideband LNAs are summarized in Table 2 for comparison. The proposed LNA achieved the widest bandwidth, comparable NF, gain and power consumption. To remove the technology dependency, the figure of merit (F.O.M) in [11] is modified and defined as

$$\mathrm{F.O.M} = \frac{\mathrm{Gain_{av}(dB)} \cdot \mathrm{BW(GHz)} \cdot f_{\mathrm{center}}(\mathrm{GHz})}{[NF_{\mathrm{av}} - 1] \cdot P_{DC}(\mathrm{mW}) \cdot f_T(\mathrm{GHz})} \tag{3.17}$$

where $\mathrm{Gain_{av}}$ is the average gain, BW is the bandwidth, f_{center} is the center frequency, $\mathrm{NF_{av}}$ is the average noise figure and $\mathrm{P_{DC}}$ is the DC power. The proposed LNA's F.O.M. exhibits a factor of 2.1 over the best previously reported result in [2] for the low cost CMOS/BiCMOS technologies.

CHAPTER IV

SUMMARY AND CONCLUSION

The design of ultra-wideband LNA in the 20-57 GHz band is described in this thesis. The LNA employs the frequency-controlled positive-negative feedback technique to enhance the gain flatness and expand the 3dB bandwidth in MMW frequency. The current-reused technique is utilized to reduce the overall power consumption. The LNA is implemented using Jazz 0.18-μm BiCMOS technology. The measurement result demonstrates a flat gain of 10.5 ± 0.5 dB across 20-57 GHz bandwidth with minimum NF of 5.1 dB, input P_{1dB} higher than -19 dBm and IIP3 better than -8 dBm. The overall power consumption is 8.8 mA with the 1.8 V supply voltage. The proposed LNA shows the widest operation bandwidth with low power consumption comparing to the other MMW WB LNAs in table 2, which is very attractive for MMW wireless applications.

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